## REMARKS

Claims 1-14 were examined and reported in the Office Action. Claims 1, 2, 5 and 12-14 are rejected. Claims 1, 8, 9 and 12 are amended. New claims 15-18 are added. Claims 1-18 remain.

Applicant requests reconsideration of the application in view of the following remarks.

### I. 35 U.S.C. § 102(b)

It is asserted in the Office Action that claims 1, 2, 5 and 12-14 are rejected under 35 U.S.C. § 102(b), as being anticipated by U. S. Patent No. 6,429,679 issued to Kim et al ("Kim"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131,

> [a] claim is anticipated only if each and every element as set forth i n the claim is found, either expressly or inherently described, in a s ingle prior art reference.' (Verdegaal Bros. v. Union Oil Co. of Cali fornia, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The ele ments must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. ( In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Applicant's amended claim 1 contains the limitations of

> [a]n on-DRAM termination resistance control circuit for adjusting a resistance within a semiconductor memory device that performs an on-DRAM termination operation, comprising: push-up resistance adjusting means for adjusting resistances of a first and a second inner resistor based on an external reference resistor; pull-down resistance adjusting means for adjusting a resistance of a third inner resistor based on the second inner resistor that is adjusted by the push-up resistance adjusting means; and resistance adjustment control means for controlling the operations of the push-up resistance adjusting means and the pull-down resistance adjusting means for a predetermined commanded adjustment time, wherein the resistance adjustment control means includes a ring

> oscillator controlling means for outputting a control signal to start an operation and finish the operation for the predetermined commanded adjustment time depending on an external resistance adjust command.

Applicant's amended claim 12 contains the limitations of

> [a]n on-DRAM termination resistance control method for adjusting resistance within a semiconductor memory device that performs an on-DRAM termination operation, comprising the steps of: (a) adjusting resistances of a first and a second inner resistor based on an external reference resistor, the first and the second inner resistor used to generate a push-up code; (b) adjusting a resistance of a third inner resistor based on the second inner resistor that is adjusted at the step (a), the third inner resistor used to generate a pull-down code; and (c) controlling the steps (a) and (b) for a predetermined commanded adjustment time.

Kim discloses generating a signal for controlling the UP driver; and MOS arrays 4 and 8 are used for generating a signal for controlling the LOW driver. Distinguishable, Applicant's claimed invention asserts both first and second inner resistors 201 and 210 are used to generate a push-up code; a third inner resistor is used to generate a pull-down code (see amended claim 12 and new claim 15). The push-up code and the pull-down code are respectively input to a push-up decoder and a pull-down decoder in an interface circuit 120 for performing an on-DRAM termination operation (see Applicant's Fig. 1; specification page 7, line 26 to page 8, line 3). Therefore, Kim does not teach, disclose or suggest: Applicant's amended claim 1 limitations of

> resistance adjustment control means for controlling the operations of the push-up resistance adjusting means and the pull-down resistance adjusting means for a predetermined commanded adjustment time, wherein the resistance adjustment control means includes a ring oscillator controlling means for outputting a control signal to start an operation and finish the operation for the predetermined commanded adjustment time depending on an external resistance adjust command,

or Applicant's amended claim 12 limitations of

> the first and the second inner resistor used to generate a push-up code; (b) adjusting a resistance of a third inner resistor based on the second inner resistor that is adjusted at the step (a), the third inner resistor used to generate a pull-down code; and (c) controlling the steps (a) and (b) for a predetermined commanded adjustment time.

Since Kim does not disclose, teach or suggest all of Applicant's amended claims 1 and 12 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Kim. Thus, Applicant's amended claims 1 and 12 are not anticipated by Kim. Additionally, the claims that directly or indirectly depend from claims 1 and 12, namely claims 2 and 5, and 13-14, respectively, are also not anticipated by Kim for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(b) rejections for claims 1, 2, 5 and 12-14 are respectfully requested.

## III. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 3, 4, 6-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-14, as they now stand, are allowable for the reasons given above.

## CONCLUSION

In view of the foregoing, it is submitted that claims 1-18 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: May 1, 2006

By: _____

Steven Laut, Reg. No. 47,736

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on May 1, 2006.

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Jean Svoboda